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Amendments to the Written Description of the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

On page 1, after the title insert: --Background Of The Invention--;

On page 1, after "Background of the Invention" but before the first paragraph insert --Field of the Invention--;

On page 1, before the second paragraph beginning on line 4, insert --Discussion of the Related Art--;

Please amend the second, third and fourth paragraphs beginning on page 1, lines 4 through page 2, line 2 as shown below:

Fig. 1 schematically shows an integrated circuit 10 comprising a microprocessor (μP) 12, an internal memory (MEM) 14, and input/output terminals (I/O) 16. Microprocessor 12 is intended to execute a program or ~~a~~ software stored in memory 14. Under control of the program, microprocessor 12 can process data provided by input/output terminals 16 or stored in memory 14 and provide data through input/output terminals 16.

To check the proper operation of the microprocessor, a supervision circuit 18 (TEST) is generally integrated ~~to~~ on integrated circuit 10. Supervision circuit 18 is capable of reading specific data provided by microprocessor 12 on execution of a program, and of possibly processing the read data. Supervision terminals 22 connect supervision circuit 18 to an analysis tool 24. Analysis tool 24 may process the received signals, for example, according to commands provided by a user, and ensure a detailed analysis of the operation of microprocessor 12. In particular, analysis tool 24 may determine the program instruction sequence really executed by microprocessor 12.

The number of supervision terminals 22 for a conventional supervision circuit 18 may be on the same order of magnitude as the number of input/output terminals 16 of microprocessor 12, for example, from 200 to 400. Test terminals 22 as well as the connections of supervision circuit 18 take up a significant silicon surface area, which causes an unwanted increase in the circuit

cost. For this reason, a first version of integrated circuit 10 comprising supervision circuit 18 and supervision terminals 22 is produced in small quantities to check out microprocessor 12. After this checking out, a version of integrated circuit 10 rid of supervision circuit 18 and of supervision terminals 22 is sold. This ~~implies~~ requires the forming of two versions of the integrated circuit, which requires a significant amount of work and is relatively expensive. Further, the final chip is not identical to the tested chip.

Please amend the third and fourth full paragraphs on page 2, lines 13-29 as shown below:

Thus, standard IEEE-ISTO-5001, in preparation, provides in its 1999 version, accessible, for example, on website www.ieee-isto.org/Nexus5001, a specific message exchange protocol between a supervision circuit 18 and an analysis tool 24 for a supervision circuit 18 requiring but a reduced number of test terminals 22.

Standard IEEE-ISTO-5001 provides several standardized messages, called public messages, the features of which are set once and for all and cannot be modified by the users of chip 10. Among the public messages, program tracing messages and data messages are especially distinguished. Program tracing messages provide information relative to the order of execution of the program by microprocessor 12. It may, for example, be a message indicating that a jump has occurred in the program executed by microprocessor 12. Data messages gather the other public messages that can be transmitted by supervision circuit 18 and especially provide information relative to the data processed by microprocessor 12. It may, for example, be a message indicating that a data read or write operation in an area of memory 14 has been performed by microprocessor 12.

On page 4, before the line 4, insert --Summary of the Invention--;

Please amend the third full paragraph on page 4, lines 11-28 as shown below:

To achieve this ~~object~~ and other objects, the present invention provides a method for transmitting digital messages through output terminals of a microprocessor supervision circuit of a determined type from among several supervision circuit types integrated ~~to~~ on a microprocessor, each message comprising a message identifier and being formed of several

groups of successive juxtaposed bits, the bit groups being divided in one or several segments each comprising a determined number of bits, the method ~~consisting~~ comprising of successively transmitting segments associated with the successive juxtaposed bit groups comprising a first bit group corresponding to the identifier and comprising a fixed number of bits whatever the supervision circuit type; second bit groups, at least one of the second groups comprising a fixed number of bits depending on the identifier and on the type of supervision circuit, the number of the other second groups depending on the identifier and being independent from the supervision circuit type; a third bit group comprising a number of bits greater than one and depending on the message to be transmitted; and fourth bit groups each comprising a number of bits greater than one and depending on the message to be transmitted, the number of fourth groups depending on the identifier, on the supervision circuit type, and on the message to be transmitted.

Please amend the third paragraph on page 5, lines 7-24 as shown below:

The present invention also provides a device of digital message transmission through output terminals of a supervision circuit, of a determined type from among several supervision circuit types, integrated ~~to~~ with a microprocessor, each message comprising a message identifier, said device comprising means for providing groups of successive juxtaposed bits forming the message, means for dividing the bit groups in one or several segments each comprising a determined number of bits and means for successively transmitting said segments, the bit group provision means being capable of successively providing a first bit group corresponding to the identifier and comprising a fixed number of bits identical whatever the supervision circuit type, second bit groups, at least one of said second groups comprising a fixed number of bits depending on the identifier and on the type of supervision circuit, the number of the other second groups depending on the identifier and being independent from the supervision circuit type, a third bit group comprising a number of bits greater than one and depending on the message to be transmitted, and fourth bit groups each comprising a number of bits greater than one and depending on the message to be transmitted, the number of fourth groups depending on the identifier and on the determined supervision circuit type.

On page 5, before line 25, insert --Brief Description of the Drawings--;

On page 6, before line 3, insert --Detailed Description--;

Please amend the paragraph beginning on page 8, line 20 through page 9, line 6 as shown below:

The present invention further enables modifying the composition of the messages to be transmitted to adapt them to the customers' requirements while enabling transmission of the public messages already provided by standard IEEE-ISTO-5001. Since the position of the groups in a message is set for all the messages according to the present invention that can be transmitted by supervision circuit 18 to analysis tool 24, it is possible to standardize as much as possible the calculation algorithms of the analysis tool for the processing of the received messages. A configuration file is transmitted to analysis tool 24 so that it is acquainted ~~of~~ with the messages that can be transmitted by supervision circuit 18 and in particular that it is acquainted for each message ~~of~~ with the number of bits (possibly equal to zero) forming fixed customer group CUSTOM. On reception of a message by analysis tool 24, analysis tool 24 thus knows the position of fixed customer groups CUSTOM and can thus analyze all the data present in this group. Optional customer groups CUST_1 to CUST_N being clearly identified by analysis tool 24, they can be ignored by an analysis tool 24 which would not be capable of processing them.

On page 9, line 14, please insert:

--Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:--